Linux-driven RISC-V core to debut on an NXP i.MX SoC

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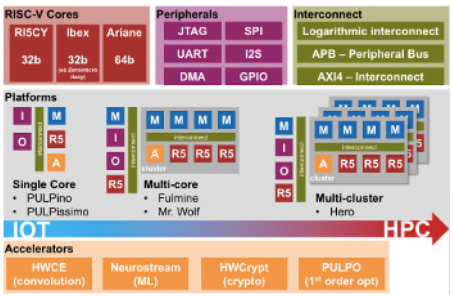

The OpenHW Group unveiled a Linux-driven ?CORE-V Chassis? eval SoC due for tape-out in 2H 2020 based on an NXP i.MX SoC, but featuring its RISC-V-and PULP-based 64-bit, 1.5GHz CV64A CPU and 32-bit CV32E cores. Meanwhile, Think Silicon demonstrated a RISC-V-based NEOX|V GPU.

A not-for-profit, open source RISC-V initiative called the OpenHW Group that launched in June has announced that it plans to tape out a Linux-friendly CORE-V Chassis evaluation SoC in the second half of 2020 built around its 64-bit CV64A CPU core and 32-bit CV32E coprocessor. The RISC-V based cores will be integrated into an undefined, NXP i.MX heterogeneous, multi-core SoC design. The SoC was announced at this week?s RISC-V Summit in San Jose, Calif., where Think Silicon also demo?d an early version of a RISC-V-based NEOX|V GPU (see farther below).

The open source CV64A CPU core and 32-bit CV32E are based on RISC-V architecture PULP Platform cores developed by the University of ETH Zurich. The 64-bit CV64A core is based on ETH Zurich?s Ariane implementation of its RV64GC RISC-V core IP. RV64GC is also used by many other RISC-V projects, including SiFive?s U54.

[2]

Linux

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